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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.

8733.20127

First Inventor or Application Identifier

Kwangjo HWANG

Title

Liquid Crystal Display Device and Method of Manufacturing the Same

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g. PTO/SB/17)
(Submit an original and a duplicate for fee processing)

2. ☒ Specification

Total Pages

12

3. ☒ Drawing(s) (35 U.S.C. 113) Total Sheets

8

4. ☐ Oath or Declaration

Total Pages

- a. ☐ Newly executed (original or copy)

- b. ☐ Copy from a prior application (37 C.F.R. §1.63(d))
(for continuation/divisional with box 15 completed)

- i. ☐ DELETION OF INVENTOR(S)

Signed statement attached deleting inventor(s) named
in the prior application, see 37 C.F.R. §1.63(d)(2) and
1.33(b).

5. ☐ Incorporation By Reference (usable if box 4B is checked)
The entire disclosure of the prior application, from which a copy of the
oath or declaration is supplied under Box 4B, is considered to be part
of the disclosure of the accompanying application and is hereby
incorporated by reference therein.

ACCOMPANYING APPLICATION PARTS

6. ☐ Assignment Papers (cover sheet & document(s))
7. ☐ 37 C.F.R. §3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
8. ☐ English Translation Document (if applicable)
9. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
10. ☐ Preliminary Amendment
11. ☒ White Advance Serial No. Postcard
12. ☐ Small Entity Statement(s) ☐ Statement filed in prior application. Status still proper and desired.
13. ☒ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
14. ☒ Other: Request for Priority
List of Inventors' Names and
Addresses

15. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no.:

Prior application information: Examiner:

Group Art Unit:

16. Amend the specification by inserting before the first line the sentence:

☐ This application is a ☐ Continuation ☐ Division ☐ Continuation-in-part (CIP)
of application Serial No. Filed on

☐ This application claims priority of provisional application Serial No. Filed

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Docket No. 8733.20127

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Kwangjo HWANG et al.

FILING DATE: Herewith

FOR: LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

LIST OF INVENTORS' NAMES AND ADDRESSES

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WASHINGTON, D.C. 20231

SIR:

Listed below are the names and addresses of the inventors for the above-identified patent application.

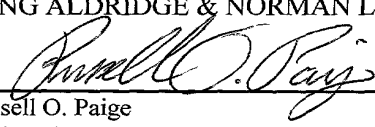
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A declaration containing all the necessary information will be submitted at a later date.

Respectfully Submitted,

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LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

Cross Reference

This application claims the benefit of Korean Patent Application No. 1999-19145,
5 filed on May 27, 1999, under 35U.S.C. §119, the entirety of which is hereby incorporated by
reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display device, and more particularly
10 to a liquid crystal display device fabricated through four photolithography processes and a
method of fabricating the same.

Description of the Related Art

As shown in Figure 1, a typical liquid crystal display (LCD) device has a gate bus
15 line 60 arranged in a transverse direction and a data bus line 70 arranged in a longitudinal
direction, a thin film transistor (TFT) formed near a cross point of the gate bus line 60 and the
data bus line 70. The TFT has a source electrode 70a, a drain electrode 70b, a gate electrode
60a, and a semiconductor layer 80. The drain electrode 70b is connected to a pixel electrode
40.

20 The LCD device described above is completed through five photolithography
processes.

Hereinafter, a method of fabricating the conventional LCD device will be explained
in detail. Figures 2A to 2E show a process of manufacturing the conventional LCD device,
and Figures 3A and 3B show a photolithography process to form a gate insulating layer 50,
25 the amorphous silicon (a-Si) layer 80a, and an n-type impurity doped silicon (n^+ a-Si) layer

80b. Further, Figures 4A - 4C show a photolithography process to form source and drain electrode 70a and 70b.

First, a gate electrode 60a shown in Figure 2A is formed on a transparent substrate 10 during a first photolithography process.

5 In the first photolithography process, a metal layer (not shown) of Mo or Cr is deposited on the transparent substrate 10 and then a photoresist is applied on the metal layer. Then, a first photo-mask (not shown) is located over the substrate 10, and light exposure and developing processes are performed to etch the metal layer so that the gate electrode 60a is formed. Finally, the photoresist remaining on the metal layer is removed, leaving the gate electrode 60a on transparent substrate 10 as shown in Figure 2A.

Second, a gate insulating layer 50, the a-Si layer 80a, and a n^+ a-Si layer 80b shown in Figure 2B are sequentially formed during a second photolithography process, detailed as shown in Figures 3A and 3B.

As shown in Figure 3A, a photoresist 88 is applied on the n^+ a-Si layer 80b. After that, light exposure and developing processes are performed using a second photo-mask 100, thereby forming a photoresist pattern 88a as shown in Figure 3B. The a-Si layer 80a and the n^+ a-Si layer 80b are simultaneously etched according to the photoresist pattern 88a so that the gate insulating layer 50, the a-Si layer 80a, and the n^+ a-Si layer 80b are formed. Finally, the photoresist remaining on the n^+ a-Si layer 80b is removed.

20 Third, the source electrode 70a and the drain electrode 70b shown in Figure 2C are formed during a third photolithography process, detailed as shown in Figures 4A - 4C.

As shown in Figure 4A, a metal layer 170 such as Cr is deposited over the whole surface of the substrate 10 while covering a-Si layer 80a and n^+ a-Si layer 80b. After that, the positive type photoresist 88 is applied, and then light exposure and developing processes are performed using a third photo-mask 200, thereby forming a photoresist pattern 88a as shown

in Figure 4B. In accordance with the photoresist pattern 88a, a lower metal layer 170 is etched to form the source electrode 70a and the drain electrode 70b as shown in Figure 4C. Continually, the n^+ a-Si layer 80b is etched using the metal layer (source and drain electrodes) as a mask. Finally, the photoresist pattern 88a remaining on the source electrode 70a and the drain electrode 70b is removed.

Fourth, the passivation layer 55 having the contact hole 30 shown in Figure 2D is formed during a fourth photolithography process.

An inorganic material such as a nitride or oxide of silicon (SiN_x or SiO_x , respectively) or an organic material such as bis-benzocyclobutene (BCB) is deposited on the source electrode 70a and the drain electrode 70b. After that, the positive type photoresist (not shown) is applied, and then light exposure and developing processes are performed using a fourth photo-mask (not shown) to form a photoresist pattern. Then, the passivation layer 55 is formed through an etching process. After the etching process, the photoresist pattern remaining on the passivation layer 55 is removed.

Fifth, the pixel electrode 40 to be connected to the drain electrode 70b shown in Figure 2E is formed during a fifth photolithography process.

A metal layer such as indium tin oxide (ITO) is deposited on the passivation layer 55. After that, the positive type photoresist (not shown) is applied, and then light exposure and developing processes are performed using a fifth photo-mask (not shown), thereby forming a photoresist pattern. In accordance with the photoresist pattern, the metal layer is etched so that the pixel electrode 40 is formed. After the etching process, the photoresist pattern remaining on the pixel electrode 40 is removed.

The photolithography process described above includes the steps of: cleaning a substrate; applying a photoresist; soft-baking the photoresist; aligning a photo-mask; light-exposing the photoresist; developing the photoresist; inspecting the array substrate; hard-

baking the photoresist; etching a portion that the photoresist does not cover; inspecting the array substrate; and removing the photoresist.

Since the photolithography process includes the complex steps described above, as the number of photolithography processes increases, the inferiority rate become greater, leading to a low yield. In other words, reliability of the manufacturing process varies inversely proportional to the number of photolithography processes performed.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a liquid crystal display device fabricated through four photolithography processes.

Another object of the present invention is to increase yield and to reduce the production cost of TFT fabrication.

To achieve the above objects, the present invention provides a method of manufacturing a liquid crystal display device including a first photolithography process forming a gate electrode on a substrate; a second photolithography process including: a) depositing sequentially a gate insulating layer, first and second semiconductor layers, and a metal layer; b) applying a first photoresist on the metal layer; c) aligning a first photo mask with the substrate; d) light exposing and developing the first photoresist to produce a first photoresist pattern; e) etching the metal layer using a first etchant, the first etchant ashing the first photoresist pattern on a predetermined portion of the metal layer to produce a second photoresist pattern, thereby exposing the predetermined portion of the metal layer; and f) etching the gate insulating layer, the first and second semiconductor layer, and the predetermined portion of the metal layer using a second etchant according to the second photoresist pattern to form source and drain electrodes, an ohmic contact layer, and an active area; a third photolithography process forming a passivation film and a contact hole; and a

fourth photolithography process forming a pixel electrode contacting with the drain electrode through the contact hole.

The first etchant contains Cl_2/O_2 gas and the second etchant contains SF_6/HCl or $\text{SF}_6/\text{H}_2/\text{Cl}_2$ gas. The source and drain electrodes are made of a metal selected from a group consisting of Cr, Mo, Al, and Al alloy, and the first semiconductor layer comprises an amorphous silicon and the second semiconductor layer comprises an amorphous silicon doped with n-type impurity.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which like reference numerals denote like parts, and in which:

Figure 1 is a plan view of a conventional liquid crystal display device;

Figures 2A to 2E are cross sectional views taken along line I-I of Figure 1 showing a process of fabricating the conventional liquid crystal display device;

Figures 3A and 3B are cross-sectional views illustrating a photolithography process corresponding to Figure 2B;

Figures 4A to 4C are cross-sectional views illustrating a photolithography process corresponding to Figure 2C;

Figures 5A and 5B, 6A to 6E, 7A and 7B, and 8A to 8C are cross sectional views showing a process of fabricating a liquid crystal display device according to a preferred embodiment of the present invention; and

Figure 9 is a plan view illustrating the liquid crystal display device according to the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the preferred embodiment of the present invention, example of which is illustrated in the accompanying drawings.

As shown in Figure 5A, in a first photolithography process, first, a metal layer 160 of Mo or Cr is deposited on a transparent substrate 10. After that, a positive type photoresist (photosensitive layer) 88 is applied on the metal layer 160, and then a first photo-mask 15 is aligned. In the first photo-mask, a region 15a represents a light shielding area and a region 15b represents a light transmitting area.

Referring to Figure 5B, a gate electrode 60a is formed by etching the metal layer 160 according to a photoresist pattern 88a produced after light exposure and development of the photoresist 88. After that, the photoresist 88a remaining on the gate electrode 60a is removed.

In a second photolithography process, as shown in Figure 6A, a gate insulating layer 50 comprising an inorganic material such as SiN_x and SiO_x, an a-Si layer 80a, an n⁺ a-Si layer 80b, and a single or multi-layered metal layer 170 made of a metal such as Cr, Mo, Al, and Al alloy are sequentially formed on the gate electrode 60a. After that, a positive type photoresist 88 is applied on the metal layer 170 and then a second photo-mask 25 partially executing a diffraction light exposure is aligned. At this time, a region 25a represents a light shielding area, a region 25b represents a light transmitting area, and a region 25c represents a diffraction light exposing area.

Further, as shown in Figure 6B, a photoresist pattern 88a is formed by the second photo-mask 25. The region 25a is relatively thick and the region 25c is relatively thin in thickness. Further, the region 25b is completely removed so that a surface of the metal layer 170 is exposed. Specifically, the thickness of the photoresist pattern depends on a pattern shape of the second photo-mask 25.

Continually, as shown in Figure 6C, the metal layer 170 is etched by subjecting the

array substrate 10 having the photoresist pattern 88a to a first etchant containing Cl_2/O_2 gas. When an etching process for the metal layer is completed, a central portion of the photoresist pattern 88a is removed by O_2 gas ashing, thereby exposing a central portion of the metal layer 170 corresponding to the central portion of the photoresist pattern 88a.

5 And then, as shown in Figure 6D, the a-Si layer 80a and the n^+ a-Si layer 80b are etched by a second etchant preferably containing either SF_6/HCl or $\text{SF}_6/\text{H}_2/\text{Cl}_2$ gas. At this time, the metal layer 170 functions as a mask.

Further, the exposed portion of the metal layer 170 and the central portion of the n^+ a-Si layer 80b corresponding to the exposed portion of the metal layer 170 are etched by a third etchant preferably containing Cl_2/O_2 gas, thereby forming an ohmic contact layer, and source and drain electrodes 70a and 70b. At this time, the photoresist pattern 88a functions as a mask.

Subsequently, as shown in Figure 9, by the diffraction light exposure as the inventive second photolithography process, the line edge of the source and drain electrodes 70a and 70b and the line edge of the semiconductor layer 80 are formed in the shape of curved lines. The dimension "d" represents a distance between the data bus line 70 and the semiconductor layer 80 or the drain electrode 70b and the semiconductor layer 80. Since the distance 'd' is maintained equally throughout, it is possible to prevent the distance difference due to misalignment during the photolithography process.

20 In a third photolithography process, as shown in Figure 7A, an inorganic material such as SiN_x and SiO_x or an organic material such as BCB is deposited on the source and drain electrodes 70a and 70b to form a passivation layer 55. After that, the positive type photoresist 88 is applied on the passivation layer 55, and then light exposure and developing processes are executed using a third photo-mask 35, thereby forming a photoresist pattern 25 88a. In the third photo-mask 35, a region 35a represents a light shielding area and a region

35b represents a light transmitting area. Further, in accordance with the photoresist pattern 88a, as shown in Figure 7B, the passivation layer 55 is etched to form a contact hole 30 and then the photoresist pattern remaining on the passivation 55 is removed.

In a fourth photolithography process, as shown in Figure 8A, a metal layer 140 made of ITO is deposited on the passivation layer 55 having the contact hole 30. After that, the positive type photoresist 88 is applied on the metal layer 140, and then the light exposure and developing processes are executed using a fourth photo-mask 45, thereby forming a photoresist pattern 88a. In the fourth photo-mask 45, a region 45a represents a light shielding area and a region 45b represents a light transmitting area. Further, in accordance with the photoresist pattern 88a, as shown in Figure 8B, the metal layer 140 is etched so that the pixel electrode 40 is formed. After etching process, the photoresist pattern 88a remaining on the pixel electrode 40 is removed as shown in Figure 8C.

Accordingly, the substantially important components of liquid crystal display device according to the preferred embodiment of the present invention are completed by four photolithography processes described above.

In the present invention, since the a-Si layer 80a, the n^+ a-Si layer 80b and the source and drain electrodes are simultaneously formed through the same photolithography process, that is, by the diffraction light exposure using the second photo-mask, it is possible to manufacture the LCD device through the four lithography processes, thereby increasing the yield and reducing the production cost by decreasing the inferiority rate due to many photolithography processes.

It is further understood by those skilled in the art that the foregoing description is a preferred embodiment of the disclosed device and that various changes and modification may be made in the invention without departing from the spirit and scope thereof.

What is claimed is:

1. A method of manufacturing a liquid crystal display device, comprising:
 - a first photolithography process forming a gate electrode on a substrate;
 - a second photolithography process including:
 - a) depositing sequentially a gate insulating layer, a semiconductor layer, and a metal layer;
 - b) applying a first photoresist on the metal layer;
 - c) aligning a first photo mask with the substrate;
 - d) light exposing and developing the first photoresist to produce a first photoresist pattern;
 - e) etching the metal layer using a first etchant, the first etchant ashing the first photoresist pattern on a predetermined portion of the metal layer to produce a second photoresist pattern, thereby exposing the predetermined portion of the metal layer; and
 - f) etching the gate insulating layer, the semiconductor layer, and the predetermined portion of the metal layer using a second etchant according to the second photoresist pattern to form source and drain electrodes, an ohmic contact layer, and an active area;
 - a third photolithography process forming a passivation film and a contact hole; and
 - a fourth photolithography process forming a pixel electrode connecting with the drain electrode through the contact hole.
2. The method of claim 1, wherein the first etchant includes Cl_2/O_2 gas.
3. The method of claim 2, wherein the second etchant includes SF_6/HCl gas.

4. The method of claim 2, wherein the second etchant includes $\text{SF}_6/\text{H}_2/\text{Cl}_2$ gas.
5. The method of claim 1, wherein the semiconductor layer includes first and second semiconductor layers.
6. The method of claim 5, wherein the first semiconductor layer includes amorphous silicon.
7. The method of claim 5, wherein the second semiconductor layer includes doped amorphous silicon.
8. The method of claim 1, wherein the source and drain electrodes are made of a metal selected from a group consisting of Cr, Mo, Al, and Al alloy.
9. The method of claim 8, wherein the semiconductor layer includes first and second semiconductor layers.
10. The method of claim 9, wherein the first semiconductor layer includes amorphous silicon.
11. The method of claim 9, wherein the second semiconductor layer includes doped amorphous silicon.
12. The method of claim 1, wherein the pixel electrode includes indium tin oxide.

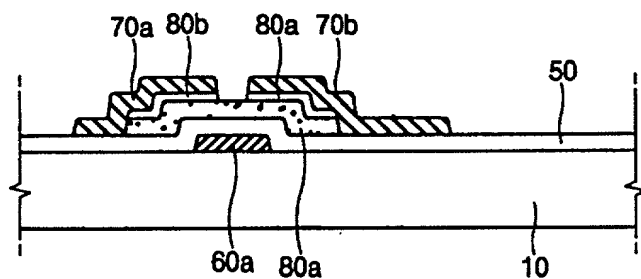
13. The method of claim 12, wherein the semiconductor layer includes first and second semiconductor layers.

14. The method of claim 13, first semiconductor layer includes amorphous silicon.

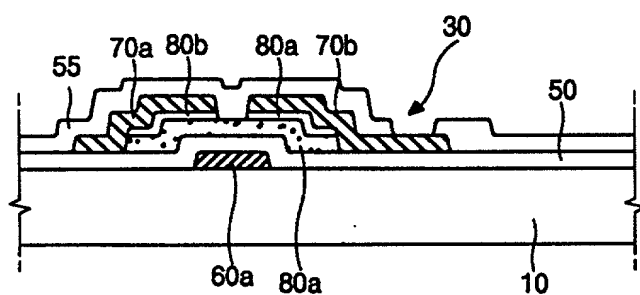
15. The method of claim 13, wherein the second semiconductor layer includes doped amorphous silicon.

ABSTRACT OF THE DISCLOSURE

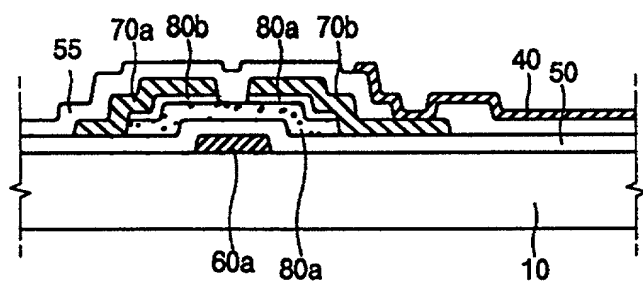
The present invention discloses a method of manufacturing a liquid crystal display device including a first photolithography process forming a gate electrode on a substrate; a second photolithography process including: a) depositing sequentially a gate insulating layer, first and second semiconductor layers, and a metal layer; b) applying a first photoresist on the metal layer; c) aligning a first photo mask with the substrate; d) light exposing and developing the first photoresist to produce a first photoresist pattern; e) etching the metal layer using a first etchant, the first etchant ashing the first photoresist pattern on a predetermined portion of the metal layer to produce a second photoresist pattern, thereby exposing the predetermined portion of the metal layer; and f) etching the gate insulating layer, the first and second semiconductor layer, and the predetermined portion of the metal layer using a second etchant according to the second photoresist pattern to form source and drain electrodes, an ohmic contact layer, and an active area; a third photolithography process forming a passivation film and a contact hole; and a fourth photolithography process forming a pixel electrode connecting with the drain electrode through the contact hole.



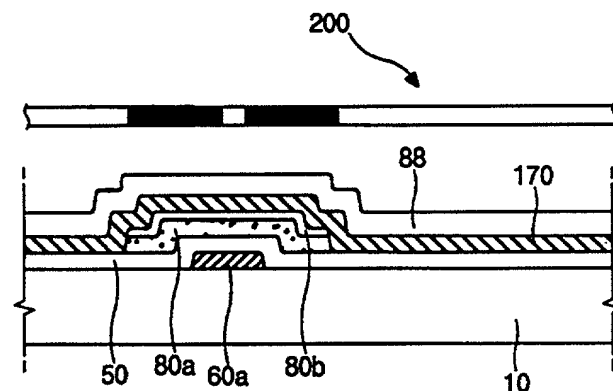
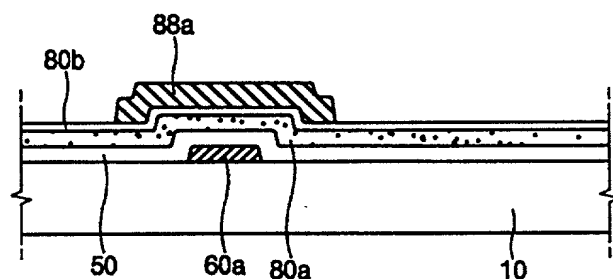
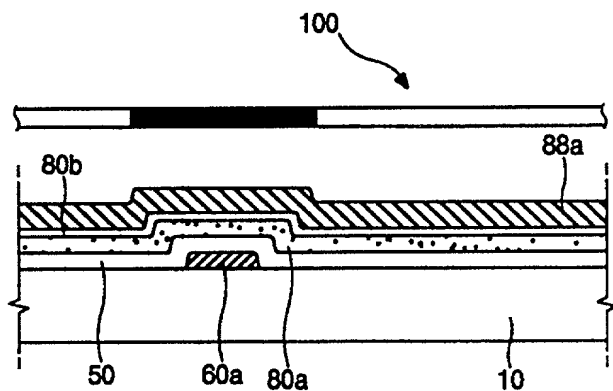
(RELATED ART)
FIG. 2C

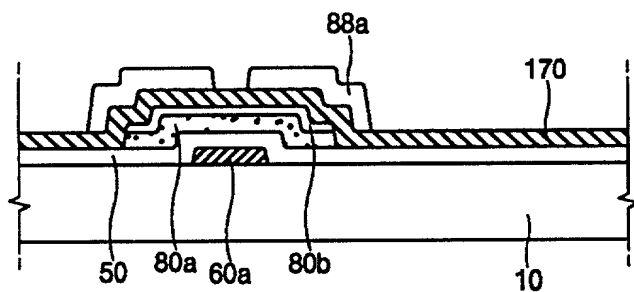


(RELATED ART)
FIG. 2D

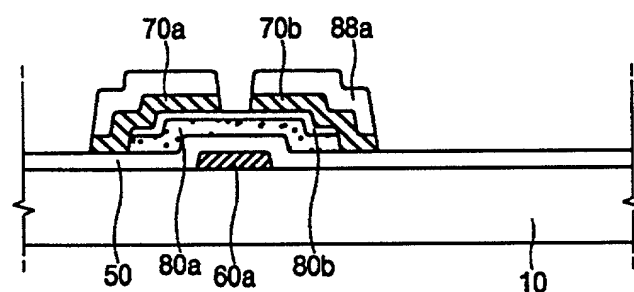


(RELATED ART)
FIG. 2E





(RELATED ART)
FIG. 4B



(RELATED ART)
FIG. 4C

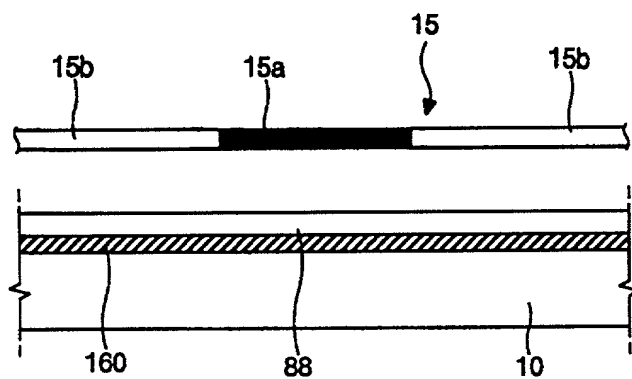
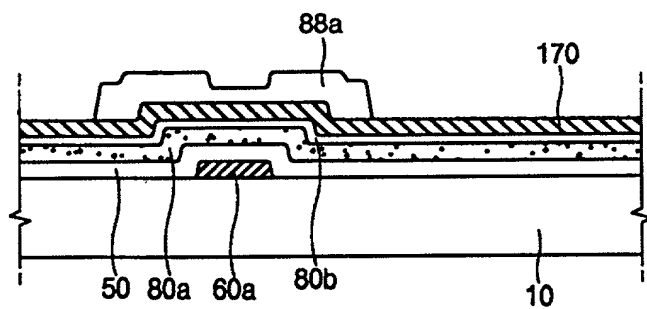
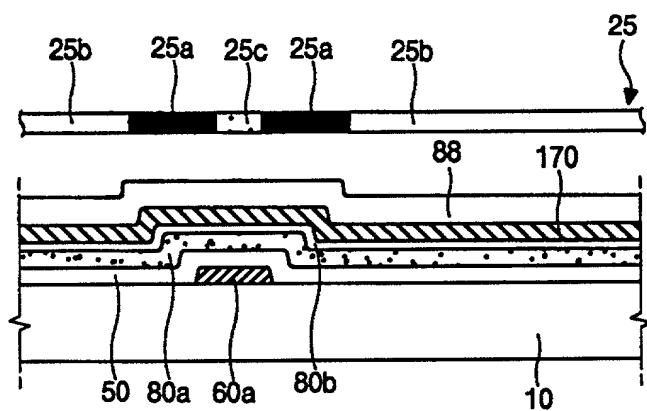
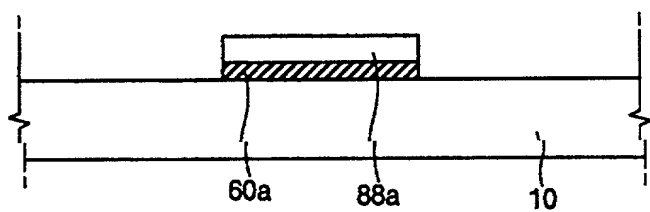


FIG. 5A



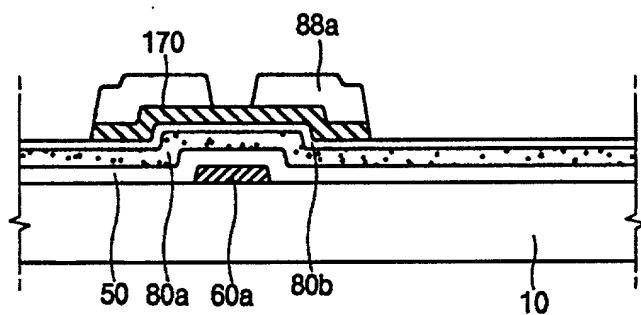


FIG. 6C

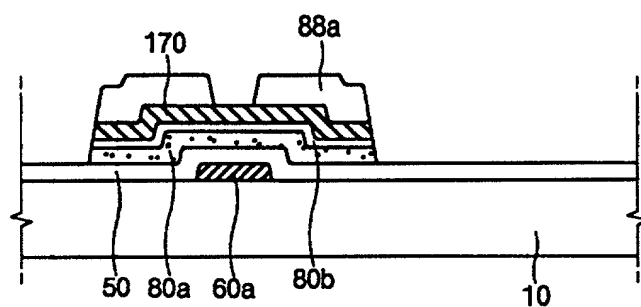


FIG. 6D

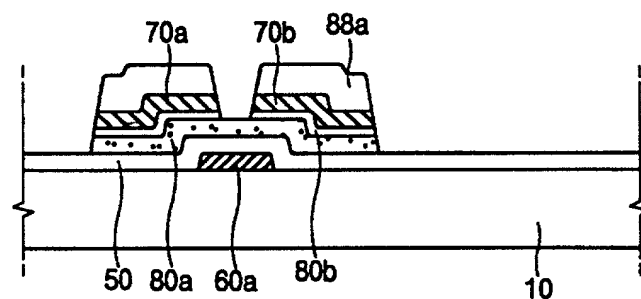


FIG. 6E

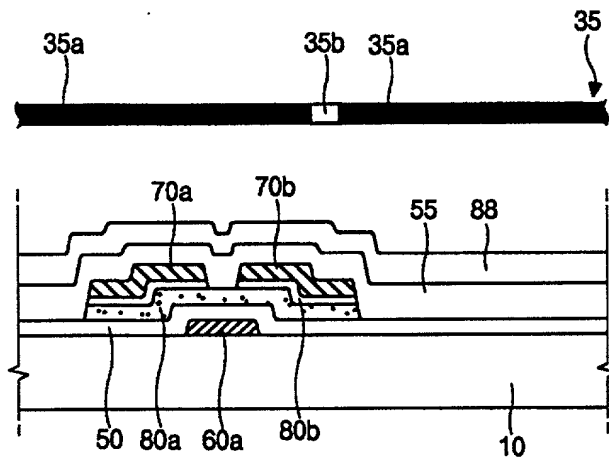


FIG. 7A

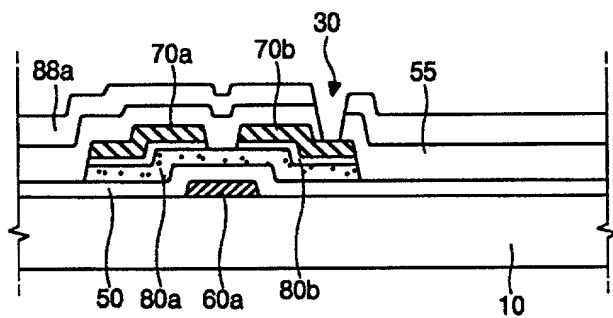


FIG. 7B

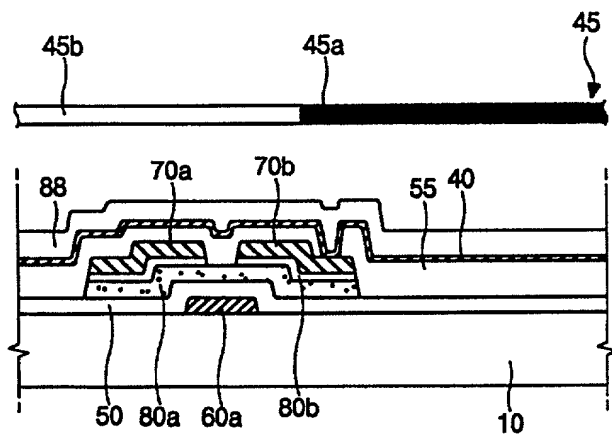


FIG. 8A

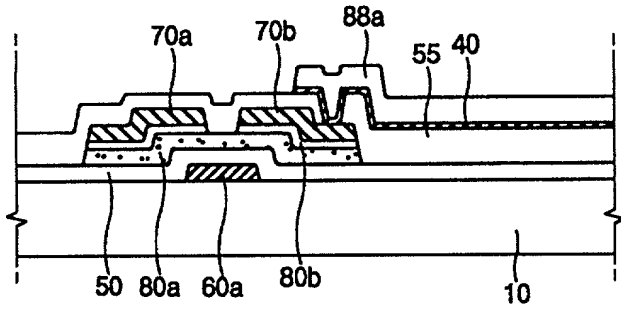


FIG. 8B

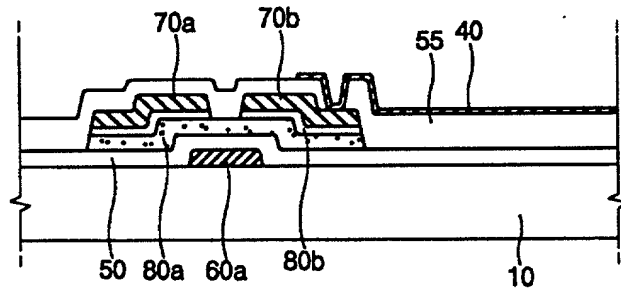


FIG. 8C

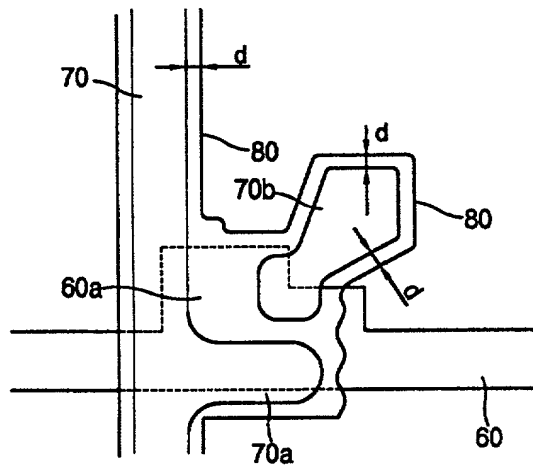


FIG. 9